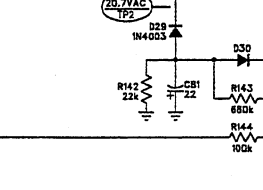
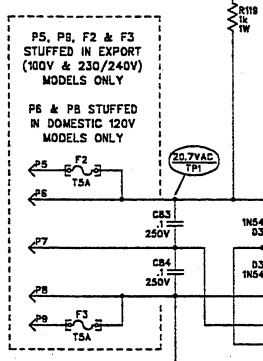
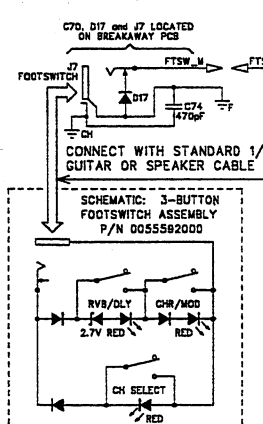
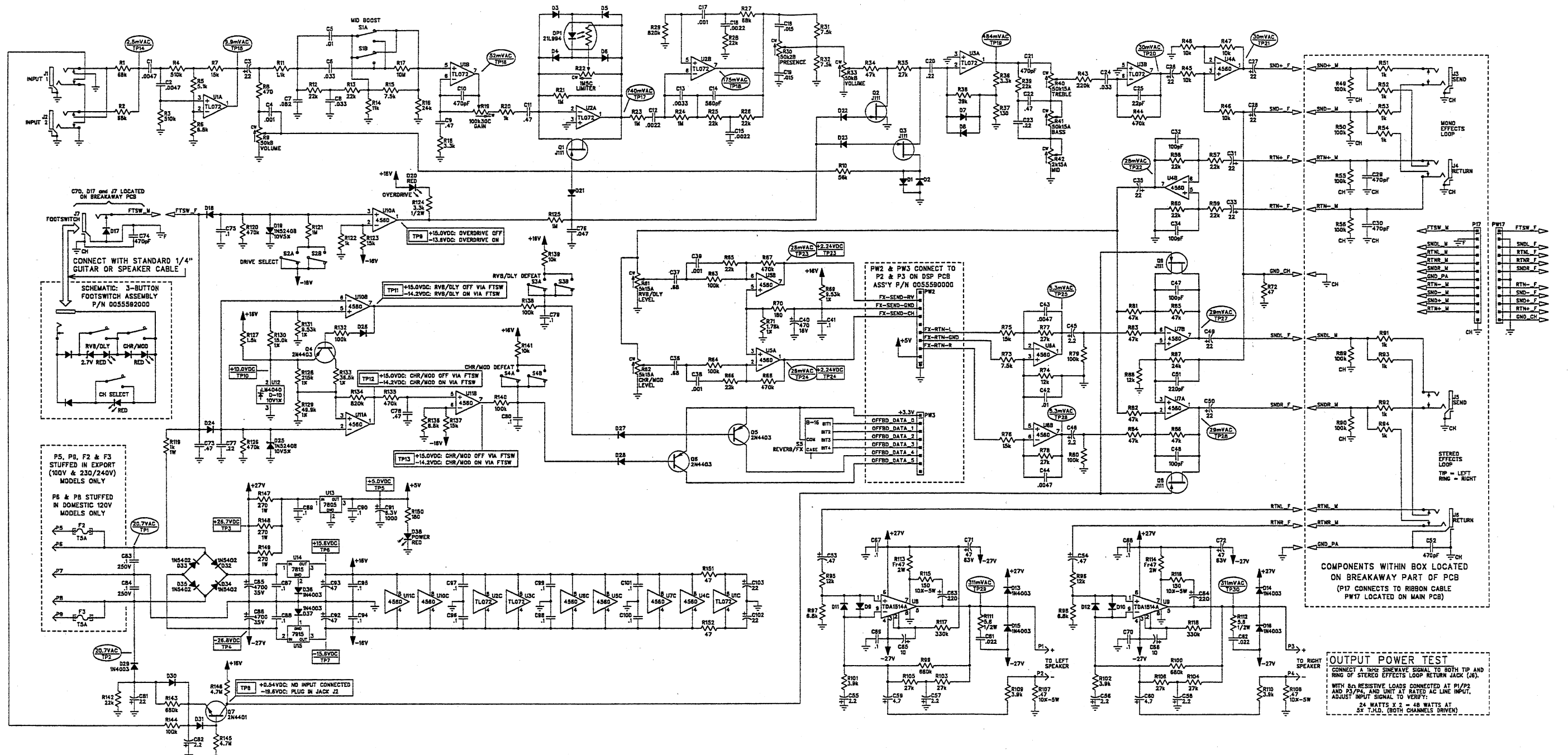


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OUTPUT POWER TEST
 CONNECT A 1KHZ SINEWAVE SIGNAL TO BOTH TIP AND RING OF STEREO EFFECTS LOOP RETURN JACK (J6).
 WITH 8Ω RESISTIVE LOADS CONNECTED AT P1/P2 AND P3/P4, AND UNIT AT RATED AC LINE INPUT, ADJUST INPUT SIGNAL TO VERIFY:
 24 WATTS X 2 = 48 WATTS AT 5% T.H.D. (BOTH CHANNELS DRIVEN)

- LAST REFERENCE DESIGNATORS: C184, D38, F3, J7, DP1, P17, Q9, R152, R15, TP30, U15, W2. (ALSO USED: PW2, PW3, PW17.)
- TESTPOINT VOLTAGES TP14-30 READ TO GROUND WITH A DVM UNDER THE FOLLOWING CONDITIONS:
 UNIT AT RATED LINE VOLTAGE
 CABLE P1/P2 CONNECTED TO P2 ON DSP PCB ASSEMBLY
 CABLE P1/P3 CONNECTED TO P3 ON DSP PCB ASSEMBLY
 P/N 005559000
 8Ω RESISTIVE LOADS (2) CONNECTED AT P1-P4
 NO FOOTSWITCH CONNECTED
 MID BOOST SWITCH OUT
 OVERDRIVE SELECT SWITCH IN
 REVERSE FX DEFEAT AND CHORUS DEFEAT SWITCHES OUT
 ALL ROTARY CONTROLS SET TO 12 O'CLOCK
 DSP PCB ASSEMBLY P/N 005558000 AND 005559000
 (REFER TO SCHEMATIC P/N 005558000 FOR TEST MODE)
- TESTPOINT VOLTAGES TP1-13 READ TO GROUND WITH A DVM AND NO INPUT SIGNAL WITH UNIT AT RATED LINE VOLTAGE AND CABLE P1/P2 CONNECTED TO HEADER P17.
- THIS SCHEMATIC IS FOR PCB FABRICATION P/N 0055578000 AND PCB ASSEMBLY P/N 005558000 AND 005559000.
- ALL DIPDES ARE 184448.
- ALL POLARIZED CAPACITORS IN μF, 20% 50V MINIMUM.
- ALL UNPOLARIZED CAPACITORS IN μF, 10% OR BETTER; 50V MINIMUM. (POWER SUPPLY BYPASS CAPACITORS ARE 20%.)
- ALL RESISTORS IN OHMS, 5% 1/4W.

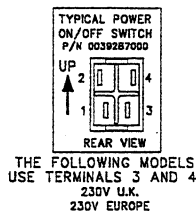
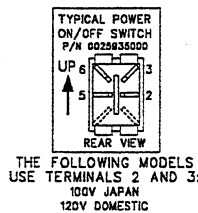
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 2621 Research Drive
 Corona, CA 91720 USA

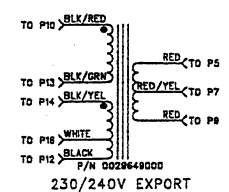
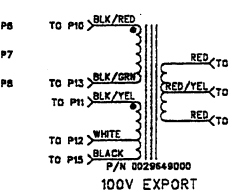
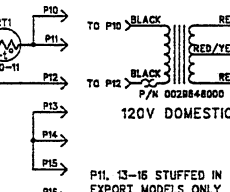
CHECKED BY: *B.Pen*
 DATE: 31-MAR-99
 APPROVED BY: *[Signature]*
 DATE: 31-MAR-99
 DRAWN: B. DESI
 ENGR: B. DESI
 DATABASE FILE: 2424S.SCH

TITLE: SERVICE DIAGRAM, COMBINED (schematic)
 PRINCETON CHORUS DSP
 MAIN PCB

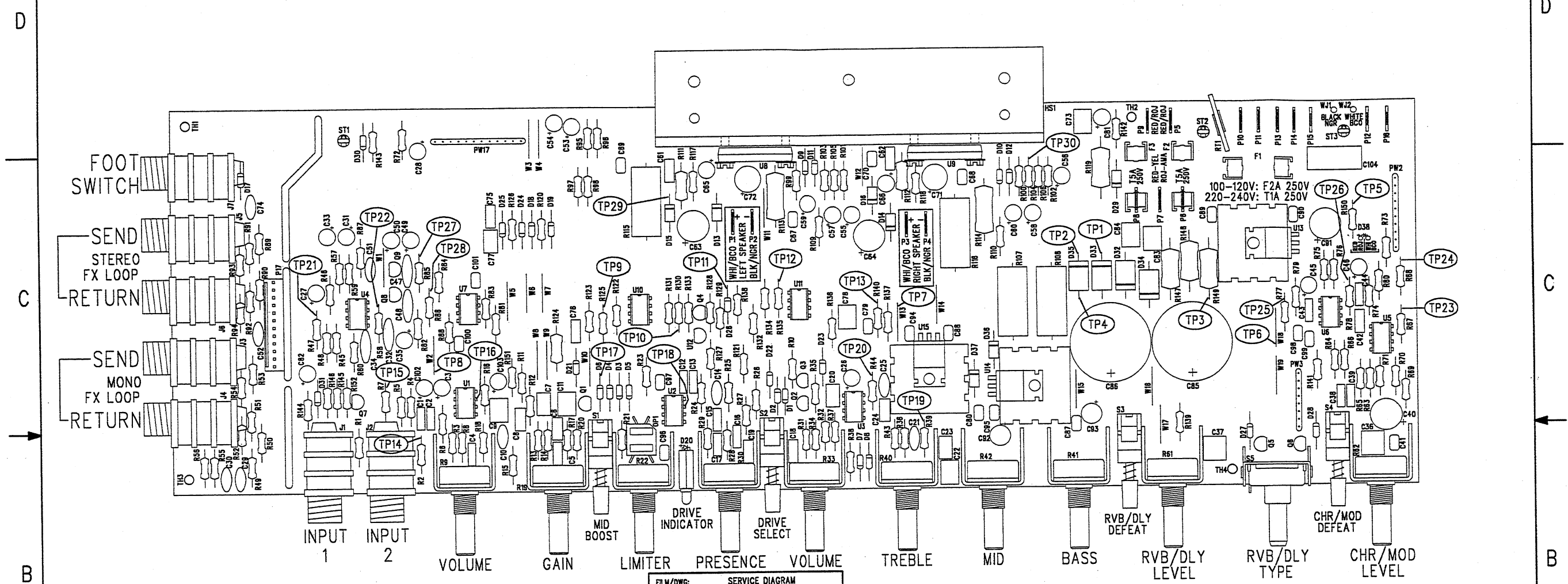
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 DRAWING NUMBER: 0055578000
 RELEASE DATE: 31-MAR-99
 SHEET: 1 OF 2



MODELS:	F1 VALUE:
100-120V	F2A 250V
230-240V	T1A 250V




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FILM/DWG: SERVICE DIAGRAM
 DATABASE: Z424P.PCB DATE: 31-MAR-99

2. DSP ASSEMBLY P/N 0055590000 MUST BE CONNECTED TO PW2 FOR SIGNAL TO APPEAR AT TP25 AND TP26.
 1. SEE SHEET 1 FOR PRIMARY WIRING, TEST CONDITIONS AND TESTPOINT VALUES.

NOTES: (UNLESS OTHERWISE NOTED)

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CHECKED BY: <u>B. Desi</u>	DATE: <u>31-MAR-99</u>	TITLE: SERVICE DIAGRAM, COMBINED (PCB assy) PRINCETON CHORUS DSP MAIN PCB	
APPROVED BY: <u>[Signature]</u>	DATE: <u>31-MAR-99</u>	SIZE: <u>C</u>	DRAWING NUMBER: <u>0055578000</u>
DRAWN: B. DESI	ENGR: B. DESI	RELEASE DATE: 31-MAR-99	SHEET 2 OF 2
DATABASE FILE: Z424P.PCB			REV. <u>A</u>